Please replace the paragraph beginning at page 16, line 1 with the following paragraph:

The entropy coding block 106 may generate an output video bitstream (e.g., OUT) in response to an intermediate signal (e.g., INT1), an intermediate signal (e.g., INT2) and an intermediate signal (e.g., INT3). The processing circuit 102 may generate the signal INT1 in response to a processed video signal (e.g., PV1). The signal PV1 may be generated by the processing circuit 104. The processing circuit 102 may also generate a signal (e.g., INT4) and may receive a signal (e.g., PMB). The signal PMB may be referred to as a prediction (or predictor) macroblock that may be received from the processing block 104. The prediction macroblock PMB may be used by the processing circuit 102. The processing circuit 104 may generate the signal INT2, the signal INT3, the signal PV1 and the signal PMB in response to the signal INT4 and an input video signal (e.g., VIDEO_IN). One bit of the signal INT3 ~~INT2~~ may be presented as a flag (e.g., CIPF). The flag CIPF may represent a constrained intra prediction flag (to be discussed in more detail in connection with FIGS. 5 ~~2~~ and 6 ~~3~~). The processing circuit 102 may also receive a control signal (e.g., CTR1). Similarly, the processing circuit 104 may receive a control signal (e.g., CTR2).